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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,902	08/21/2003	Cheng-Ming Yih	4425-315	6430

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,902	YIH ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication app ars on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *1-5,7-14 and 16-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 12/10/2003 is acceptable.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference character(s) mentioned in the description: Fig. 1D, reference 110.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. The claims are objected to because of the following informalities:

- Claim 1, line 3, "a plurality of isolation region" should be "a plurality of isolation regions"

- Claim 1, line 5, "said isolation region" should be "said isolation regions"

- Claim 1, line 7, "a plurality of gate structure" should be "a plurality of gate structures"

- Claim 2, line 1, "said isolation region" should be "**each of** said isolation regions"

- Claim 3, line 2, "said isolation region" should be "said isolation regions"

- Claim 4, line 1, "said gate structure" should be "**each of** said gate structures"

- Claim 5, line 1, "a plurality of contact" should be "a plurality of contacts"

- Claim 7, line 1, "a plurality of drain region" should be "a plurality of drain regions"

- Claim 8, line 3, "said isolation region" should be "said isolation regions"

- Claim 9, line 3, "a plurality of isolation region" should be "a plurality of isolation regions"

- Claim 9, line 4, "a plurality of gate structure" should be "a plurality of gate structures"

- Claim 9, line 7, "a plurality of drain region" should be "a plurality of drain regions"

- Claim 10, line 1, "said isolation region" should be "**each of** said isolation regions"

- Claim 11, line 2, "said isolation region" should be "said isolation regions"

- Claim 12, line 1, "said gate structure" should be "**each of** said gate structures"

- Claim 13, line 1, "a plurality of contact in" should be "a plurality of contacts **on**"

- Claim 14, line 4, "a plurality of isolation region" should be "a plurality of isolation regions"

- Claim 16, line 2, "said isolation region" should be "said isolation regions"

- Claim 17, line 1, "said isolation region" should be "**each of** said isolation regions"

- Claim 18, line 1, "a plurality of gate structure" should be "a plurality of gate structures"

- Claim 19, line 1, "said gate structure" should be "**each of** said gate structures"

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1-2, 4-7, 9-10, 12-14, and 17-19** are rejected under 35 U.S.C. 102(b) as being anticipated by Lee U.S. Patent 6,372,564.

Lee discloses in Figures 1 through 3 and respective portions of the specification a structure of nonvolatile memory array as claimed.

Referring to independent **claim 1**, Lee discloses a structure of nonvolatile memory array, comprising:

a substrate (100, Fig. 3);

a plurality of isolation regions (102, Fig. 1 and column 3, lines 3-6) in said substrate;

a buried conductive region (embedded source line SL in Fig. 1, "buried source line" 120 in Fig. 2B, column 3, lines 6-10 and lines 57-60) between said isolation regions, wherein said buried conductive region (SL or 120) is perpendicular to said isolation regions (102, best seen in Fig. 1); and

a plurality of gate structures (130, Fig. 2F) on said substrate.

Referring to independent **claim 9**, Lee discloses a structure of nonvolatile memory array, comprising:

a substrate (100, Fig. 3);

a plurality of isolation regions (102, Fig. 1 and column 3, lines 3-6) in said substrate;

a plurality of gate structures (130, Fig. 2F) on said substrate.

a buried source line (SL in Fig. 1, 120 in Fig. 2B, column 3, lines 6-10 and lines 57-60) between said isolation regions, wherein said buried source line (SL or 120) is perpendicular to said isolation regions (102, best seen in Fig. 1); and

a plurality of drain regions (142) in said substrate.

Similarly as detailed above and with reference to independent **claim 14**, Lee discloses a source line structure of a nonvolatile memory array, comprising:

a substrate (100, Fig. 3);

a plurality of isolation regions (102) in said substrate; and

a buried conductive region (SL or 120) between said isolation regions, wherein said buried conductive region (SL or 120) is perpendicular to said isolation regions (102).

Regarding **claims 2, 10, and 17**, Lee further discloses that each of said isolation regions is shallow trench isolation (STI, column 3, lines 3-5).

Referring to **claim 18**, as mentioned above, Lee further discloses a plurality of gate structures (130, Fig. 2F) on said substrate.

Regarding **claims 4, 12, and 19**, Lee further discloses that each of said gate structures comprises at least a polysilicon layer (138, column 4, lines 35-40).

Regarding **claims 5 and 13**, Figs. 1 and 2F further depict a plurality of contacts (146) on said substrate.

Regarding **claim 6**, as mentioned above, said buried conductive region (SL or 120) is a source line.

Regarding **claim 7**, as mentioned above, Lee further discloses a plurality of drain regions (142) in said substrate.

5. **Claims 1-4, 6-12, and 14-20** are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. U.S. Patent 6,153,471.

Lee et al. disclose in Figures 1 through 4 and respective portions of the specification a structure of nonvolatile memory array as claimed.

Referring to independent **claim 1**, Lee et al. disclose a structure of nonvolatile memory array, comprising:

a substrate (100, Fig. 1A);

a plurality of isolation regions (108a, Figs. 1D and 1F) in said substrate;

a buried conductive region (118, Figs. 1D, 1F, and 4B) between said isolation regions, wherein said buried conductive region is perpendicular to said isolation regions (best seen in Fig. 1D); and

a plurality of gate structures (124a/126/128, Fig. 1F) on said substrate.

Referring to independent **claim 9**, Lee et al. disclose a structure of nonvolatile memory array, comprising:

a substrate (100, Fig. 1A);

a plurality of isolation regions (108a, Figs. 1D and 1F) in said substrate;

a plurality of gate structures (124a/126/128, Fig. 1F) on said substrate.

a buried source line (118, 118 is electrically connected to source/drain 120a as depicted most clearly in Fig. 1D and detailed in column 3, lines 53-54 and lines 64-65) between said

isolation regions, wherein said buried source line is perpendicular to said isolation regions (best seen in Fig. 1D); and

a plurality of drain regions 120a ("source/drain regions") in said substrate.

Similarly, with reference to independent **claim 14**, Lee et al. disclose a source line structure of a nonvolatile memory array, comprising:

a substrate (100);

a plurality of isolation regions (108a) in said substrate; and

a buried conductive region (118) between said isolation regions, wherein said buried conductive region is perpendicular to said isolation regions.

Regarding **claims 2, 10, and 17**, Lee et al. further disclose that each of said isolation regions is shallow trench isolation (STI, column 2, line 57 to column 3, line 6).

Referring to **claim 18**, as mentioned above, Lee et al. further disclose a plurality of gate structures (124a/126/128, Fig. 1F) on said substrate.

Referring to **claims 3, 6, 11, and 16**, Figures 1C, 1D and 4B depict that a depth of said buried source line (118, and as detailed above, buried conductive line 118 is electrically connected to source/drain 120a) is less than a depth of said isolation regions (108a).

Regarding **claims 4, 12, and 19**, Lee et al. further disclose that each of said gate structures (124a/126/128) comprises at least a polysilicon layer (124a or 128, column 4, lines 25-30).

Regarding **claim 7**, as mentioned above, Lee et al. further disclose a plurality of drain regions (120a) in said substrate.

Referring to **claims 8, 15, and 20**, Figures 1C, 1D and 4B, as best seen in Fig. 4B, depict that said buried conductive region (118) is on a surface of said substrate (100), such that said buried conductive region is not under said isolation region (108a).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
July 07, 2004